On page 12, lines 8-15 (indents corrected):

The buffer valid bit is a bit that may be set when an address request initiator, such as the Pentium[[7]]® Pro Processor 41 or PCI device 44, requests a transfer and it is accepted. A cycle initiated by a PCI device 44 is normally sent to the PCI target controller 62 or to another PCI device. The bit may be cleared upon completion of the cycle, indicating that the buffer is available for another address request. This bit may be set when a processor to PCI read or write cycle is initiated by the processor and may be cleared upon the write completing on the PCI bus or the read completing on the processor bus.

lines 2-9 KC 5-24-09

On page 13, lines 1-9 (indents corrected):

This bit may be set when the response agent (e.g.: target of the address request) needs to take action. It can be cleared when the response agent is finished performing its task. This bit may be set, for example, when the Pentium processor 41 has written data to the matched data buffer for a processor-to-PCI write cycle and cleared when the data has been written from the data buffer to the PCI bus. In addition, this bit may be set immediately for a processor-to-PCI read and cleared when read data has been returned from the PCI bus to the appropriate data buffer.

On page 14, lines 5-14 to page 15, lines 1-8 (indents corrected):

Transfer Type Bit 0: **(Processor Write)**

This bit may be set when the processor initiates a write and is cleared when the processor has finished writing data to the data buffer.

Transfer Type Bit 1: **(PCI Write)**

This bit may be set when an initiator requests a PCI write cycle and is cleared when all write data has been transferred to PCI bus.

Transfer Type Bit 2: **(Processor Read)**

This bit may be set when the processor initiates a read and is cleared when the read data is returned from the matched data buffer to the processor.

Transfer Type Bit 3: **(PCI Read)**

This bit may be set when an initiator requests a PCI read cycle and is cleared when PCI read data has been returned to the data buffer.